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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/882,624

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Ian Wylie

WYLIE 5

8470

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7590

10/18/2004

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EXAMINER

KIELIN, ERIK J


ART UNIT

PAPER NUMBER

2813

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/882,624	Applicant(s) WYLIE, IAN	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) none is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 30 December 2003 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7-11, 12-16, and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Amended independent claims 7, 12, and 17 recite the limitation "wherein the first portion of one of the source/drain region is self-aligned with at least one gate sidewall spacer" in the last two lines. There is insufficient antecedent basis for this limitation in the claim. None of claims 7, 12, and 17 provides the presence of a gate or gate sidewall spacers. Accordingly, it is unclear how the source/drain region can be aligned to a feature that does not exist.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 7-10, 12-14, 16, 17-19, and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,043,778 (Teng et al.).

Regarding claims 1, 7, 12, 17, and 21, Teng discloses a semiconductor device comprising,

a semiconductor substrate 10 having N- and P-wells 14, 16 (Fig. 7);

a gate 24 above each well in the semiconductor substrate, the gate having gate sidewall spacers 42 located along sidewalls thereof (Fig. 7);

a channel region 33 (Fig. 5A; col. 9, line 4);

a trench (32 and that portion holding the part of the isolation region 20) adjacent the channel region 33 (Fig. 3; col. 8, lines 53-58);

an isolation region 20 formed adjacent the semiconductor substrate --as further limited by instant claims 2 and 22-- and located within the trench and comprising an oxide (col. 7, line 21) -
-as further limited by instant claims 4, 9, 13, 18, and 24-- wherein the isolation region includes a first portion and a second post portion (shown as the narrower portion at the top of 20, but not labeled), wherein no structural interface exists between the first and the second portions of the isolation region, and wherein the second post portion is located over the first portion, and wherein the isolation region does not extend under the channel region 33 --as further limited by

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instant claims 3, 8, and 23 -- and wherein the isolation is between the transistors indicated by the gates **24** and thereby isolates the transistors --as further limited by instant claim 16; and

a first portion of a source/drain region **44** formed in the semiconductor substrate, and a second portion of the source/drain region **36** formed on the isolation region from polysilicon (col. 8, lines 57-58) --as further limited by instant claims 5, 10, 14, 19, and 25-- and in contact with the second post portion but not in the semiconductor substrate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 6, 11, 15, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of US Patent Application 2002/0142552 A1 (**Wu**).

The prior art of **Teng**, as explained above, discloses each of the claimed features except for forming the isolation region to extend through a transistor tub ("well").

Wu teaches each of the features of the independent claims except for the second portion contacting the post portion **114a** of the isolation. Note that the isolation region extends through the tubs/wells.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use form the isolation of **Teng** to extend through a tub/well, as taught by **Wu** in order to form a more thorough isolation between devices as shown in **Wu**.

8. Claims **27-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of Applicant's admitted prior art (**APA**).

Teng, as explained above, discloses all of the features of the instant invention except for specifically showing the interconnect and other active and passive devices.

Applicant indicates that Fig. 12 shows a conventional integrated circuit (paragraph [0022]) with interconnect **1220** and other active and passive devices and that one of ordinary skill is familiar with these additional elements (paragraph [0044]).

It would have been obvious to one of ordinary skill at the time of the invention to modify **Teng** to include known interconnect and active and passive device in order to form a functioning circuit, such as a DRAM, because it highly desired in the art to form whole integrated circuits rather than just parts which would, in isolation, be useless.

9. Claim **32** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Teng** in view of **APA**, as applied to claim **27** above, and further in view of US Patent Application 2002/0142552 A1 (**Wu**).

The prior art of **Teng**, as explained above, discloses each of the claimed features except for forming the isolation region to extend through a transistor tub ("well").

Wu teaches the features as noted above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use form the isolation of **Teng** to extend through a tub/well, as taught by **Wu** in order to form a more thorough isolation between devices as shown in **Wu**.

Response to Arguments

10. Applicant's arguments filed 30 December 2003 have been fully considered but they are not persuasive.

All of Applicant's arguments are premised upon the alleged failure of **Teng** to disclose the feature of "the first portion of one of the source/drain region is self-aligned with at least one gate sidewall spacer." Examiner respectfully disagrees. This feature is clearly shown in **Teng**, Fig. 7, reference character **44**. Applicant indicates that **44** is not self-aligned with at least one of the gate sidewall spacers **42**, but this is factually in error. The first portion of the source/drain region **44** in **Teng** is shown to be aligned with the gate sidewall spacers **42** to every extent that such alignment is shown in the instant figures. For example compare the alignment of the first source/drain portion **44** beneath sidewall spacer **42** of **Teng** with the first source/drain portion **154** beneath sidewall spacer **130** of instant Fig. 1. Accordingly, Examiner respectfully submits that there exists no merit to Applicant's argument that "**Teng** ... actually teaches just the opposite" of self-alignment of the first source/drain portion **44** beneath sidewall spacer **42**.

Regarding Applicant's allegation that the source/drain contact region **36** of **Teng** fails to be aligned with the sidewall spacers **42**. Not only is this too factually in error, it is not claimed. Although the claims are interpreted in light of the specification, limitations from the specification

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are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For at least these reasons, the arguments are not found persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
17 October 2004